Application No. 10/613,162 Docket No.: 9896-000003/US

Amendment dated July 13, 2007 Reply to Office Action of April 20, 2007

AMENDMENTS TO THE DRAWINGS

The attached "Replacement Sheets" of drawings include changes to Figures 1 and 2. The attached "Replacement Sheets," which include Figures 1 and 2, replace the original sheets including Figures 1 and 2.

Attachment: Replacement Sheets

14 JMU/kk

Application No. 10/613,162 Docket No.: 9896-000003/US Amendment dated July 13, 2007

Reply to Office Action of April 20, 2007

REMARKS

Claims 1-9 are now pending in the application. Claims 1-3 are currently

amended. Claims 6-9 are added as new. No new matter has been added, as the

amendments are supported by the specification, claims, and drawings as originally filed.

The Examiner is respectfully requested to reconsider and withdraw the rejections in

view of the amendments and remarks contained herein.

DRAWINGS

Applicant has attached revised drawings for the Examiner's approval. In the

"Replacement Sheets", Applicant has amended the term "exchange" to "switch" to

accurately define the subject-matter to which the protection scope is sought and to

correspond with the amended specification. No new matter has been added to the

drawings.

SPECIFICATION

Applicant has amended the term "exchange" to "switch" to clarify the subject-

matter to which the protection scope is sought. A person with ordinary skill will

recognize in the art that "exchange" refers to a telephone exchange, and that a "switch"

is utilized in a data communication field, which could require variable bandwidth.

Applicant respectfully submits that no new matter has been added.

15 JML/6k

Amendment dated July 13, 2007 Reply to Office Action of April 20, 2007

REJECTION UNDER 35 U.S.C. § 102

Claims 1 and 4 stand rejected under 35 U.S.C. § 102(b) as being anticipated by

Calvignac et al. (U.S. Pat. No. 4,763,321). This rejection is respectfully traversed.

Calvignac appears to relate to a method for dynamically allocating circuit slots in

frames. The frames are delimited by flags and divided into bit slots which may be used

for synchronous circuit flow or asynchronous packet flow. It should be noted that the

meaning of the term "slot" in Calvignac appears to be an assigned place in a sequence

or schedule. It thus appears to refer to a time slot in a sub-frame used for transmitting

or conceder. It that appears to refer to a time side in a cap frame accessor transmitting

the circuit flow or the packet flow (Calvignac, FIG. 2A). The term "slot" in claim 1 refers

to a socket in a microcomputer that will accept a plug-in circuit board. Specifically, it

refers to a $\underline{\text{hardware}}$ plugged in a service processing board (page 1, paragraph [0004] in

the specification originally filed).

Regarding the difference between the term "slot" in claim 1 and Calvignac,

although Calvignac appears to address dynamic allocation of bandwidth, Calvignac

relates to allocation of time slots in a sub-frame for circuit flow and packet flow. Claim 1

provides for dynamic allocation of bandwidth for a plurality of <u>hardware slots</u> plugged in

a service processing board of a switch to support multiple lower flow service processing

boards to avoid bandwidth waste (page 1, paragraph [0006] in the specification

originally filed). It can be seen from the discussion that Calvignac and claim 1 are in

totally different technical areas.

As stated above, claim 1 is directed to dynamic allocation of slot bandwidth on a

switch. Claim 1 is further directed to dynamic allocation of bandwidth through N-

16 JML/kk

Application No. 10/613.162 Docket No.: 9896-000003/US Amendment dated July 13, 2007

Reply to Office Action of April 20, 2007

selected-one devices, and each slot is connected with the N-selected-one service. The

output of each N-selected-one device is connected with the main switch module. Thus,

through controlling the N-selected-one devices being gated, the bandwidth allocated to

each of the N slots can be dynamically changed. However, Calvignac does not

anticipate, teach, or suggest the N-selected-one devices and the dynamic bandwidth

allocation to the slots, and controlling the N-selected-one devices being gated to

allocate the bandwidth to gated slots.

In view of the foregoing, Applicant respectfully submits that claim 1 defines over

the art cited by the Examiner. Likewise, claim 4 which depends from claim 1, also

defines over the art cited by the Examiner.

REJECTION UNDER 35 U.S.C. § 103

Claim 2 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over

Calvignac et al. as applied to claim 1 above and further in view of Barr ("How

Programmable Logic Works", by Michael Barr, 1999, by Miller Freeman, Inc.). Claim 3

stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Calvignac et al.

as applied to claim 1 above and further in view of Altera's data sheet. Claim 5 stands

rejected under 35 U.S.C. § 103(a) as being unpatentable over Calvignac et al. as

applied to claim 1 above and further in view of Vitesse's data sheet. These rejections

are respectfully traversed.

The arguments made above with respect to Calvignac apply equally hereto.

Further, Calvignac, individually or in combination with the additional cited art, fails to 17

JIMI 7kk

Application No. 10/613,162 Docket No.: 9896-000003/US Amendment dated July 13, 2007

Reply to Office Action of April 20, 2007

teach or suggest the rejected claims. This rejection is respectfully traversed on the

grounds that either of Barr, Altera's data sheet, or Vitesse's data sheet, like Calvignac,

does not teach or suggest the above-discussed technical features. Instead, as admitted

by the Examiner, Barr merely mentions a programmable logic chip, Altera's data sheet

at best only discloses an EPLD with type EPM7256AEQC208-10, and Vitesse's data

sheet at best only mentions the 1.25 GHz Ethernet signal driver with type VSC7132YB.

None of the cited references disclose or suggest the N-selected-one devices and the

dynamic bandwidth allocation to the slots, and controlling the N-selected-one devices

being gated to allocate the bandwidth to gated slots.

In view of the foregoing, Applicant respectfully submits that claims 2, 3 and 5

define over the art cited by the Examiner. Thus, Applicant respectfully requests

withdrawal of the rejection under 35 U.S.C §103(a).

CONCLUSION

In view of the above amendment, applicant believes the pending

application is in condition for allowance. It is believed that all of the stated grounds of

rejection have been properly traversed, accommodated, or rendered moot. Applicant

therefore respectfully requests that the Examiner reconsider and withdraw all presently

outstanding rejections. Thus, prompt and favorable consideration of this amendment is

respectfully requested. If the Examiner believes that personal communication will

expedite prosecution of this application, the Examiner is invited to telephone the

18

undersigned at (248) 641-1600.

JMUkk

Application No. 10/613,162 Docket No.: 9896-000003/US

Amendment dated July 13, 2007 Reply to Office Action of April 20, 2007

Applicant believes no fee is due with this response. However, if a fee is due, please charge our Deposit Account No. 08-0750, under Order No. 9896-000003/US from which the undersigned is authorized to draw.

Dated: July 13, 2007 Respectfully submitted,

By /Joseph M. Lafata/ Joseph M. Lafata Registration No.: 37,166 HARNESS, DICKEY & PIERCE, P.L.C. P.O. Box 828 Bloomfield Hills, Michigan 48303 (248) 641-1223 Attorney for Applicant

Attachments